

DOCKET NO. SC13135TC

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Date: April 19, 2004
To: H. Jey Tsai - 2812
Location: United States Patent and Trademark Office
Fax No.: (703) 872-9306
From: Daniel D. Hill - 35,895
Subject: 10/728,621- Yang Du

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MESSAGE:

Enclosed herewith, please find a RESPONSE TO RESTRICTION REQUIREMENT for filing in the below-identified application.

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2.	x	2 page Response to Restriction Requirement

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PLEASE GIVE THESE PAPERS TO:

EXAMINER: H. Jey Tsai
GROUP ART UNIT: 2812
SERIAL NO.: 10/728,621
FILED: DECEMBER 5, 2003
INVENTOR: YANG DU

DOCKET NO. SC13135TC

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S) Yang Du GROUP ART UNIT: 2812
APPLN. NO.: 10/728,621 EXAMINER: H. Jey Tsai
FILED: December 5, 2003
TITLE: METHOD AND CIRCUIT FOR MULTIPLYING SIGNALS WITH A
TRANSISTOR HAVING MORE THAN ONE INDEPENDENT GATE
STRUCTURE

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RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to an Office Action mailed March 24, 2004 setting a period of
response of one month.

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RESPONSE TO RESTRICTION REQUIREMENT

REMARKS

Claims 1- 41 are pending in the application. In the Office Action mailed March 24, 2004, the examiner stated that there are two distinct inventions and provided classifications for a process for making a semiconductor device (claims 1 - 30) and a semiconductor device (claims 31 - 41).

The applicants herein elect, without traverse, claims 1 - 30. Claims 31 - 41 are herein withdrawn from consideration.

Believing to have responded to the restriction requirement mailed March 5, 2004, the Applicants respectfully request the consideration and allowance of elected claims 1 - 30; thereby placing the application in condition for allowance.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Motorola, Inc.
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By:



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